Chemical mechanical planarisation (CMP) is an enabling process technology in semiconductor integrated circuit manufacturing. The current semiconductor industry association (SIA) international technology roadmap for semiconductors (ITRS) asserts that process capabilities will meet planarity and uniformity requirements up to 2020. However, to facilitate the satisfaction of these requirements, significant technical challenges must be addressed, such as the integration of polishing solutions to assure local and global control of process parameters.

This paper will provide an overview of the development of the CMP process in the semiconductor industry to date. It will also review some of the proposed solutions to the indicated current and future challenges in the process and some of the models proposed by researchers to address non uniform characteristics of the CMP process. In that regard, there will be a detailed dissertation on models of the locally varying Von Mises stresses at the pad-wafer interface and the effect that a varying Von Mises stress distribution induces on surface planarity and material removal rate.

Keywords: Chemical Mechanical Polishing, Planarisation, Damascene, Substrate, Von Mises Stress

1 INTRODUCTION

Moore’s law asserts that integrated circuit devices must follow a trend of increased density of circuitry within the unit chip to ensure increased functionality. Lithography facilitates high resolution fabrication of intricate features on a disc shaped substrate of up to 300mm diameter [1]. Lithographic patterning requires a planar surface around the immediate chip area to allow adequate resolution of the resulting patterns. The processes involved in creating a functional layer of integrated circuitry, termed a metallisation layer, are schematically illustrated in fig. 1. Current planarity achievable by CMP facilitates depth of focus requirements of lithographic patterning with $R_{a,\text{max}}$ values as low as 3 nm reported over a 60 µm position range [2].

![Fig. 1 The metallisation cycle in semiconductor device fabrication](image-url)
However, the indications of the SIA ITRS roadmap, stating the long-term anticipation that CMP will meet the necessary planarity requirements until the year 2020 [1], masks many short term challenges in the process. The ITRS roadmap cites a number of challenges for the future of CMP, not least the proposed introduction of 450 mm diameter, 800 µm thick, brittle silicon wafers and the future trends of 13 levels of metallisation on the back end damascene interconnection structure (illustrated in fig. 3 (a) below) of the devices, requiring improved planarity. Challenges also exist with the material properties of copper metal and the porous, brittle low-k dielectrics. The existence of processing induced and crystal growth related sub surface defects are also of concern. In addition to these future challenges, however, the challenge of developing a model of the holistic CMP process remains a priority [3]. The numerous considerations in attempting to develop an integrated CMP model are summarised in fig. 2.

![Fig. 2 Illustration of some of the factors to be considered in modelling the CMP Process [3]](image)

### 2 LOW-K DIELECTRIC MATERIALS

The low relative capacitance requirement for electrically insulative (dielectric) material surrounding metal interconnect wires arises to minimise the storage of charge escaping copper interconnect wires due to electro-migration. To provide a low dielectric constant, a porous material is necessary to reduce the effective capacitance [1]. Materials such as Organo-Silicate Glass (OSG), Fluoro-Silicate Glass (FSG) and Spin-On Methyl-Silses-Quioxane (MSQ) have been discussed for future inter-metal dielectric solutions [4]. With the effective dielectric constant of these materials ranging from 3.5 to less than 2, such porous, brittle materials deform at a higher rate than the adjacent metal lines [5]. The introduction of low-k materials also brings in concerns of delamination and over-polishing [2]. One possible dielectric material offering a solution to the trade off between mechanical properties and dielectric properties has been proposed [6, 7]. Here, a composite, cross linked polymeric structure consisting of a PGMEA (propylene glycol monomethyl ether acetate)
sacrificial “skeleton” material is combined with a poly-MSQ matrix material. This porogen can be mechanically processed at a high dielectric constant, followed by curing under a stimulus such as UV light to remove the PGMEA, liberating a nanoporous material of lower effective dielectric constant [4, 6]. Though this solution has yet to be realised in production, the studies of Lazzeri et al. [6] and Zenasni et al. [7] convey a detailed understanding of the by-products of the curing process and the chemical transformation kinetics experienced by the composite porogen material. The importance of this approach to lower the effective dielectric constant during processing is expected to become increasingly significant in ultra low-k (ULK) materials where a substantial k increase induced by CMP has been predicted [4, 5].

Tsujimura [2] compares available low down force planarisation technologies with CMP. Electro-Chemical Mechanical Polishing (ECMP) is considered the key contender to CMP featuring a lower down force of below 1 psi (~0.007 MPa) but limited capability to mechanically remove copper complex layers to a surface roughness $R_{a,max} = 16$nm (compared to 3nm in CMP) and at a lower polishing rate, therefore increasing the time and cost of a polish cycle.

**Fig. 3 (a)** Damascene structure **(b)** Modelling of loading induced deformation of the structure [2]

Finite element modelling of uniform loading applied to damascene structures as shown in fig. 3 indicates a maximum acceptable uniform load of 2 psi (~0.014 MPa) for the future 32nm technology node provided that the Young’s modulus (E) of the dielectric does not fall below 3.5 GPa [1, 2]. The result of this finite element modelling work is a model which may be used as a predictive tool to estimate the sub surface integrity resulting from of a particular set of mechanical force parameters in CMP.

3 INTRODUCTION OF 450mm WAFERS BY 2012

The challenge in increasing wafer diameter within the semiconductor industry is evident; to incorporate machinery designed to effectively handle and process larger diameter wafers [1]. Further challenges await in 450mm wafers due to increased sag at the centre of the wafer. The principal causes of sag are cited as increased weight and increased surface film stresses, inducing larger
bending tendencies as illustrated in fig. 4 [8]. Calculations by Watanabe and Kramer indicated the 
required dimensional scaling of 450 mm wafers to maintain the maximum 136 µm sag tolerance for 
300mm wafers. They advocated increases in thickness based on mathematical bending expressions 
given in [8]. To correct for the increased weight, a thickness of 2.25 times the current thickness of 
300mm wafers (775 µm) would be required, i.e. a 1744 µm thick wafer. Similarly, a 1.5 times 
increase to 1163 µm would account for the increased radius-dependent film stresses [8]. The 
increase thickness in both cases serves to improve the rigidity of the wafer against bending stresses.

Focusing on the edge defect shown in fig. 4, estimates by Witt and Cook [9] indicate that the 
current 3mm edge exclusion zone creates a loss of approximately 2699 mm² of pure silicon in CMP 
of 300mm wafers. Based on a chip size of 10mm x 12 mm and a cost of US$100 per chip, this 
would equate to US$2,200 potential revenue lost per wafer [9]. This current 3mm edge exclusion 
zone reported in CMP is accountable for a large loss in potential revenue per wafer and must be 
scaled to ensure the effect does not continue to increase the number of chips affected as devices of 
smaller feature size are developed. The optical profilometry in fig. 5 illustrates the waviness 
associated with the surface of the overpolished edge region. The 3mm defective edge annulus in the 
100mm wafer analysed in fig. 5 represents a wafer surface area of 11.64 % upon which no chips 
may be fabricated. Assuming the current 300mm wafer edge region thickness of 1% of the wafer 
diameter is maintained (i.e. a 4.5mm thick edge exclusion zone for 450mm wafers), a 3.96% loss of 
available surface area would result. However, this equates to 6,298 mm² of Si, indicating a potential 
revenue loss of US$5,200 per 450mm wafer if the same costs cited by Witt and Cook are assumed 
[8]. Significant cost increases result from creating lower crystal defect silicon in a new solidification 
mechanism with an 8 day cycle for creating one 2,100mm length 450mm diameter ingot [8]. The 
revenue potential per unit surface area of silicon is also increasing due to the 45nm and 32nm 
feature size chips [1]. The importance of developing a solution to reduce this edge defect zone is 
thus evident.

4 KEY PERFORMANCE INDICES (KPIs) IN CMP

To analyse the performance of a given CMP process, there are many parameters to be 
considered in terms of achieving efficient, effective and economic planarisation. Since the process
involves removing material from a substrate, the material removal rate (RR) is one of the KPI’s, expressed in Å.min⁻¹ (1 Å = 10 nm). A high material removal rate is generally desired in any manufacturing operation but must be balanced with surface topography reduction by removing only the necessary quantity of material from the peaks of the surface topography. The productivity drive outlined in [1] indicates that another KPI in CMP is the time taken to complete one polish cycle, i.e. polish time, where a short polish time implies a larger number of wafers can be processed in a given unit of time.

As the process is termed planarisation, the extent of planarity achieved is certainly a KPI. It is necessary, therefore, to analyse the post-process topography. Four length scales are of interest in analysis of the maximum non-uniformity post-CMP. These scales are particle scale, feature scale, chip / die scale, and wafer scale. At particle scale, the non-uniformity within a single feature is of interest. This within feature non uniformity (WIFNU) quantity may be measured in terms of surface roughness variables such as $R_a$, rms roughness ($R_q$) and peak-to-valley roughness ($R_{a,max}$). Feature scale non uniformity is a measurement of local planarity within a chip or a “die”. This Within Die Non Uniformity (WIDNU) is also generally discussed in terms of such parameters as $R_{a,max}$ etc.

Die scale uniformity refers to the extent to which one chip / die deviates from the other and is therefore a global planarity parameter. By comparing the non-uniformity within a certain number of dies on the wafer surface, an overall within wafer non uniformity (WIWNU) value is given by:

$$ WIWNU = Max \left[ \frac{|WIDNU_{i+1} - WIDNU_i|}{\sum_i WIDNU} \right] \times 100 $$

where $i$ is a given location on the wafer surface and $i+1$ is the next chosen location. This WIWNU expresses the maximum measured within die non uniformity (WIDNU) as a fraction of the sum of all measured dielectric thickness deviations. WIWNU can be measured from any number of points on a wafer surface but a large number of uniformly distributed points will yield a more accurate representation of the wafer than a small number of points chosen at random.

When measuring non-uniformity at die scale, the extent which this non-uniformity figure can be repeated should also be accounted for, incorporating a 4th parameter at wafer scale, termed wafer to wafer non uniformity (WTWNU), where the reliability of the CMP process is tested by its ability to generate a wafer scale non-uniformity within an acceptable limit and within a specified tolerance of the previous wafer so that consistency of output is guaranteed.

5 QUANTIFYING AND MODELLING NON-UNIFORMITY IN CMP

Optical profilometry analysis was performed on a 100mm silicon wafer patterned with Aluminium interconnect wires and Silicon Dioxide Inter Layer Dielectric (ILD) to quantify the extent of within die non uniformity. The sample analysed was fabricated in a process predating the damascene process, known as ILD CMP, whereby the roles of the metal and dielectric illustrated in fig. 1 are reversed, i.e. ILD is removed and ILD thickness would be measured to quantify WIWNU. The optical profilometry image in figure 5 above displays feature scale uniformity in the edge exclusion zone of the 100mm sample. Figure 6 demonstrates the reduced waviness, or increased order, of the surface in the centre region. In this sample, however, the feature size indicates a prior
generation device, polished with a Logitech CDP tool for just 60 seconds. As indicated by Tsujimura, current levels of process optimisation allow for $R_{a,\text{max}} = 3\text{nm}$ within a die area [2].

![Image 1](image1.png)

**Fig. 6** Optical Profilometry showing within die uniformity near the wafer centre

![Image 2](image2.png)

**Fig. 7** Schematic illustration of the wafer carrier mechanism in CMP

Wang *et al.* [10] developed a finite element model of CMP where the material removal rate was observed to sharply peak at the edges of the wafer. This effect was attributed to the down force exerted on the entire carrier mechanism, shown in fig. 7, where the design shown causes this entire force to be exerted on the outer retaining ring. The magnitude of this down force is thought to affect friction in accordance with principles of the elastohydrodynamic lubrication regime of fluid flow applicable to the behaviour of the slurry film in CMP [10]. However, Wang *et al.* [10] and Morimoto *et al.* [11] report that the down force pressure alone does not affect non uniformity significantly [10, 11]. Results published by Wang *et al.* illustrate that the compliance of the carrier film exerting back pressure on the wafer is significant, both in small non uniformity variations from centre to edge, and in the magnitude of non uniformity at the edge [10]. It is concluded that the von Mises stress distribution at the pad/wafer interface correlates to the resulting non uniformity.

Merchant *et al.* contest this conclusion, focusing their work on the film stress induced non uniformity with the conclusion that, although von Mises stress augments the effects of wafer curvature, the effect of von Mises stress disappears completely in the absence of wafer bending [12]. The work of Fu and Chandra [14] prescribes an optimisation of wafer surface pressure by control of wafer backside loading, stating that by loading the wafer edges in tension and the centre in compression, i.e. under vacuum, a uniform pressure distribution is delivered to the pad wafer interface. Given this wafer curvature, the work by Wang *et al.* [10] modelling the von Mises stress distribution demonstrates that a lower compliance carrier film will yield a reduction in non-uniformity. Fu and Chandra also highlight the misconception that uniform carrier loading will result in uniform interface pressure, thus highlighting a requirement for variable compliance of the carrier film for variable loading such that the interface pressure is constant [3,14].
The models proposed by Sundararajan et al. [17] and Mullany et al. [18] differ to those documented above. Sundararajan et al. developed a two dimensional model to describe a 2D hydrodynamic CMP configuration. Mullany et al. extended this work to model the changeability of slurry viscosity with changes in process temperature thus facilitating estimation of the effective hydrodynamic pressure which bears some of the load applied by the wafer carrier in CMP [18]. On the other hand, research presented by Wang et al. [13] focused on the input particle size distribution of the abrasive slurry particles, prescribing which of the abrasives participate in material removal, thus indicating which proportion of abrasives affect the effective interfacial contact area and von Mises stresses.

A further difference arises from the approach taken in the model of copper CMP developed by Paul et al. [19]. In this work, the influence of mechanical factors is discussed in the context of the reaction mechanism with a low mechanical forces system favouring the formation of these species but mechanically harsh conditions likely to discourage these surface reactions from taking place. A high dependency on the high initial rate of chemical reaction for the copper oxidation process is thus deduced from this work [19].

Though the models discussed above focus on different aspects of CMP, all models may be represented by mathematical equations [10, 12, 13, 14, 17, 18, 19]. An integrated solution for CMP may be deduced from the diagnosis offered in [2, 10, 13, 14, 18, 19]. By maintaining a pressure lower than 2 psi at all locations on the substrate surface, no deformation will be caused by the CMP process, provided all substrate materials satisfy $E \geq 3.5\text{ GPa}$ [2]. Wang et al. indicates a need for higher compliance acting on the backside of the wafer. Fu and Chandra illustrate the importance of variable carrier film compliance to obtain a uniform pressure distribution at the wafer surface [14]. The work of Wang et al. establishes an expression for the effective contact area between the substrate surface and the active abrasives, which bear the remainder of the load applied by the wafer carrier [13]. Mullany et al. [18] and Levert et al. [20] establish the hydrodynamic pressure profile under the wafer, thus facilitating estimation of the load bearing potential of the fluid. The work of Paul et al. highlights the chemical action in CMP and its dependence on lower mechanical forces [19].

6 CONCLUSIONS

Significant progress has been achieved in the CMP process capabilities, maintaining the pace set by other fabrication technologies in semiconductor device manufacturing. Planarisation capabilities of as little as 3nm maximum surface roughness variation within a chip have been achieved [2] featuring 45nm average size nanopatterns on a large 300mm substrate processed in a single polish step. This progress has been facilitated by considerable development of new assemblies, mechanisms and process conditions in CMP. However, the development of an integrated model for the CMP process has not yet been completed, though many models have been developed.

In order to maximise the applicability of CMP in the semiconductor manufacturing industry, an increase in the scientific based development of optimised solutions and components is imperative in reducing yield loss and the cost of ownership of CMP equipment to maximise utilisation.
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