

# Random Noise: Our Old Foe but New Friend in Achieving High-Performance Frequency Synthesis

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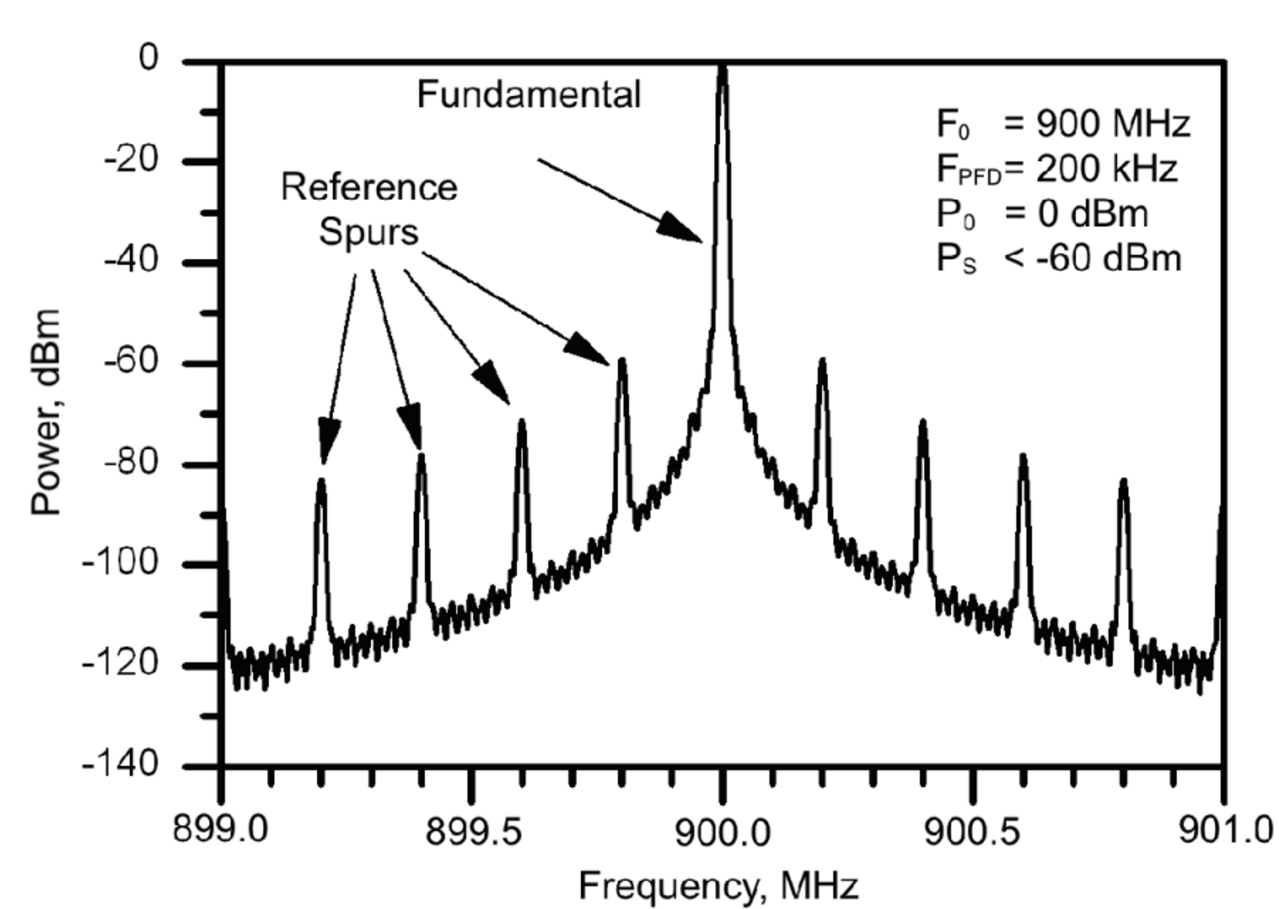
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## Introduction

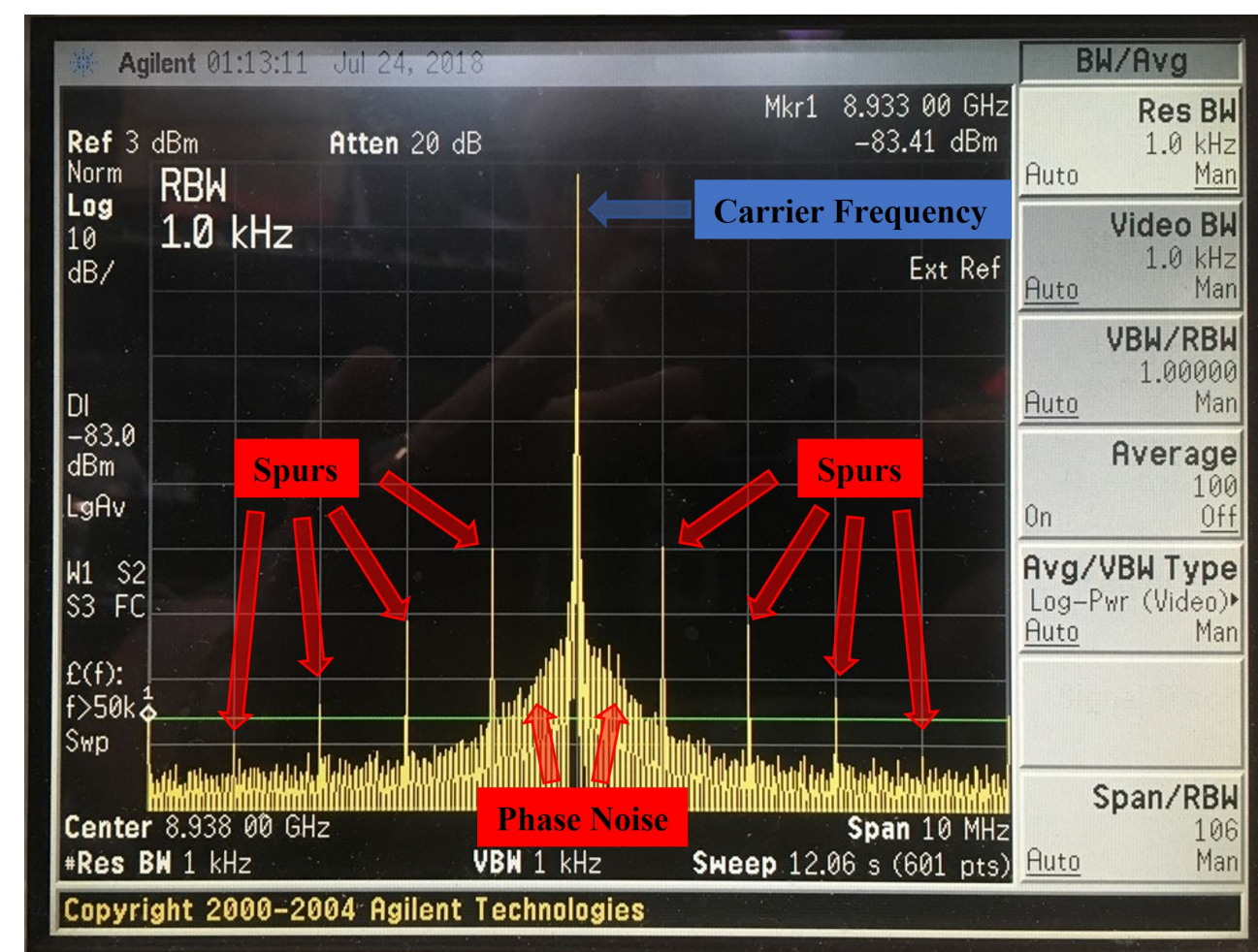
In communication systems, frequency synthesizers (FS) are used in both transmitter and receiver to generate a (relatively high-frequency) carrier signal to convey the (relatively low-frequency) information signal in a dedicated communication channel centered at the carrier frequency.

Ideally, the synthesized carrier needs to be a very high frequency, e.g., the 900 MHz and 8.9 GHz synthesized frequencies, where  $1\text{M}=10^6$  and  $1\text{G}=10^9$ , as shown below, that is **stable and clean** in the spectrum. However, these desired features are indeed hard to achieve simultaneously. There are two key phenomena that can arise in FS that undermine the overall spectral performance of the system, namely

- ✗ **phase noise (PN)**: noise spectrum adjacent to the carrier signal, arising due to the **intrinsic random noise sources** within the FS;
- ✗ **spurious tones** or **spurs**: undesired tones synthesized close to the carrier, arising due to the **periodic signal patterns** within the FS.



(a) Simulated FS spectrum example.

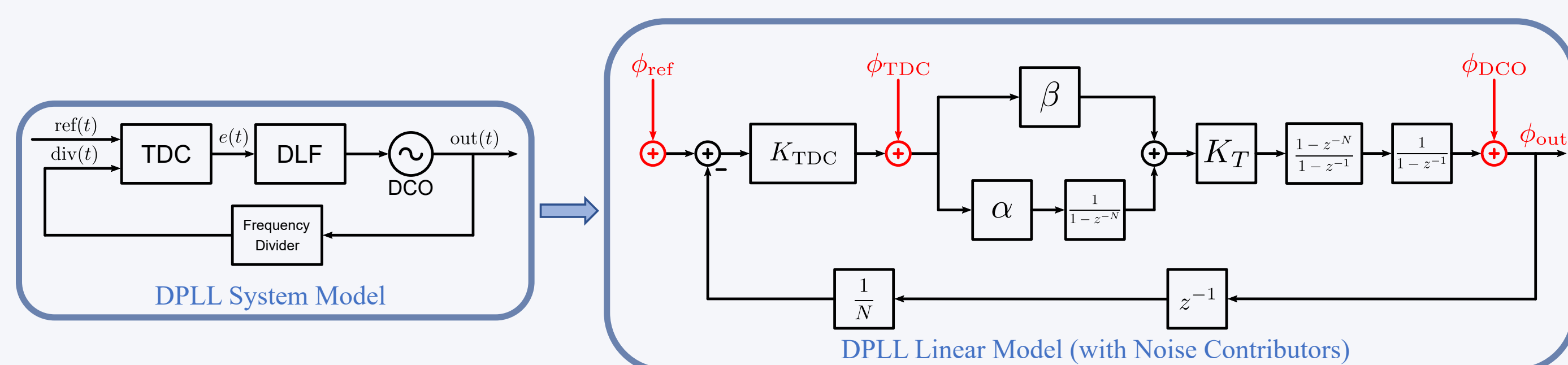


(b) Measured FS spectrum example.

In general, certain types of spurs are considered even worse than the PN in advanced wireless communications. Are there any design tricks that we can play with to use the randomness of the PN to scramble the periodicity and achieve low-spur FS? This question has motivated ongoing research into a school of design methodologies based on the phenomenon of stochastic resonance (SR) for state-of-the-art FS systems. This work introduces our insight about the SR method and discusses its potential to achieve even higher-performance FS.

## Stochastic Resonance in Digital Frequency Synthesizer

The digital phase locked loop (DPLL) is becoming more and more popular to be used as advanced radiofrequency synthesizer.



Three sources contribute to its noise performance, namely the reference and digitally controlled oscillator (DCO) jitters and the time-to-digital converter (TDC) quantization error. The former two are random noises, and the latter is periodic because the TDC's output must periodically bounce among several quantization levels in the steady state.

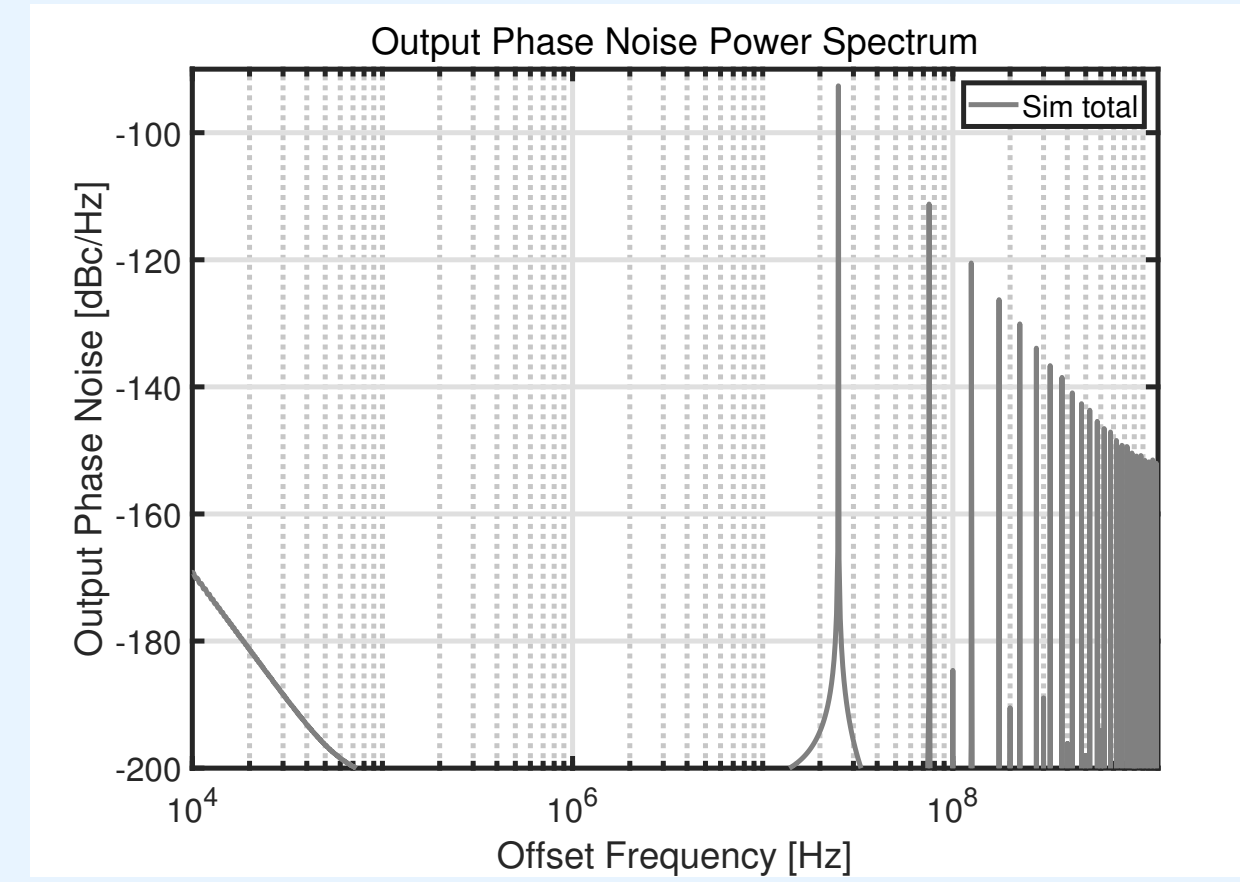
To achieve SR in the DPLL, we use the RMS input jitter as an indicator, e.g., for the DPLL using a 1-bit TDC, that can be calculated as

$$\sigma_{\Delta t} = \frac{\eta}{2} + \sqrt{\left(\frac{\eta}{2}\right)^2 + \sigma_{t_{n,ref}}^2}, \text{ where } \eta = \sqrt{\frac{\pi}{2}} \cdot \left(\frac{N\beta K_T}{2} + \frac{\sigma_{t_{n,DCO}}^2}{2 \cdot \beta K_T}\right).$$

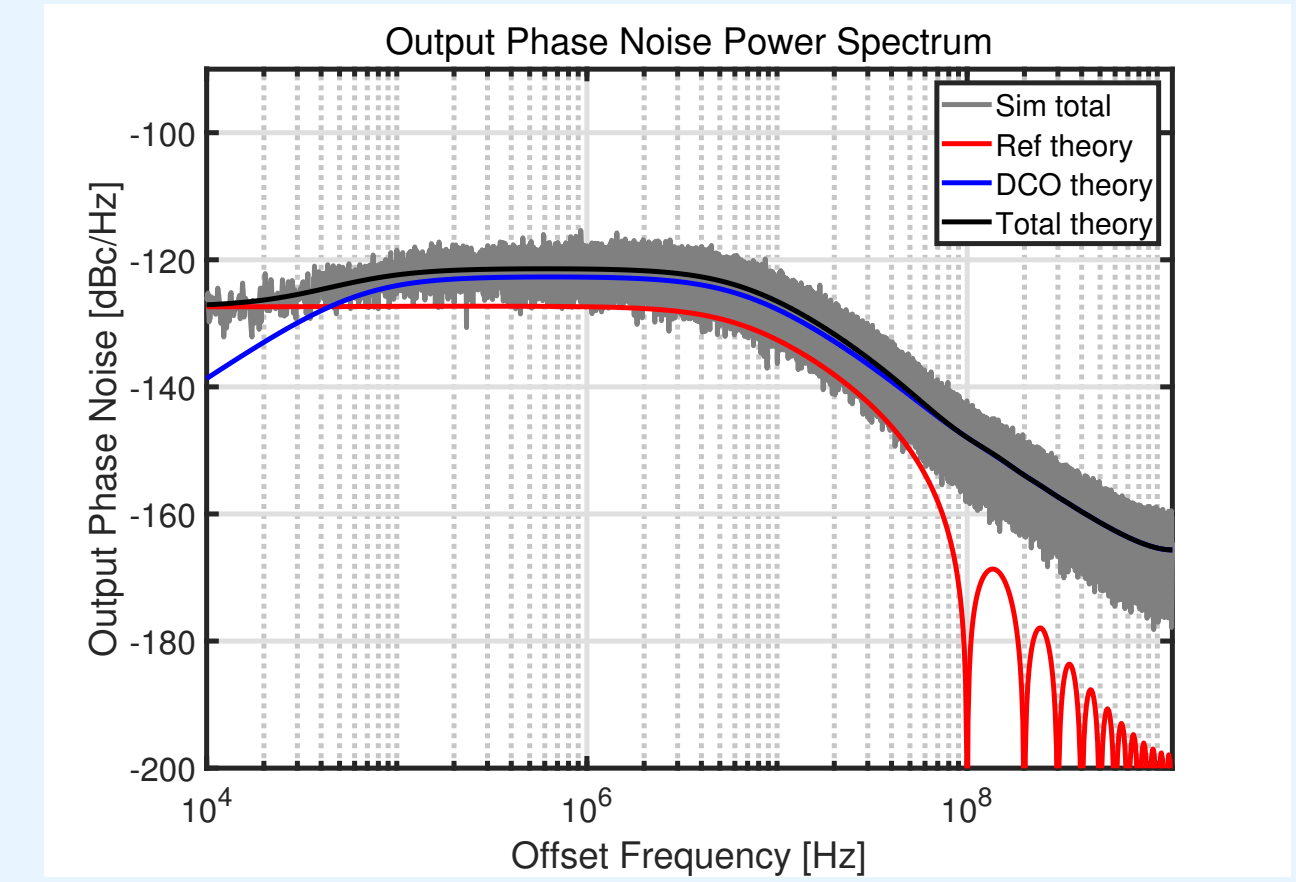
The system jitter is minimized, when the optimal  $\beta = \hat{\beta}$ , as

$$\frac{\partial \sigma_{\Delta t}}{\partial \beta} = \frac{\partial \eta}{\partial \beta} = 0, \text{ where } \hat{\beta} = \frac{\sigma_{t_{n,DCO}}}{K_T \cdot \sqrt{N}}.$$

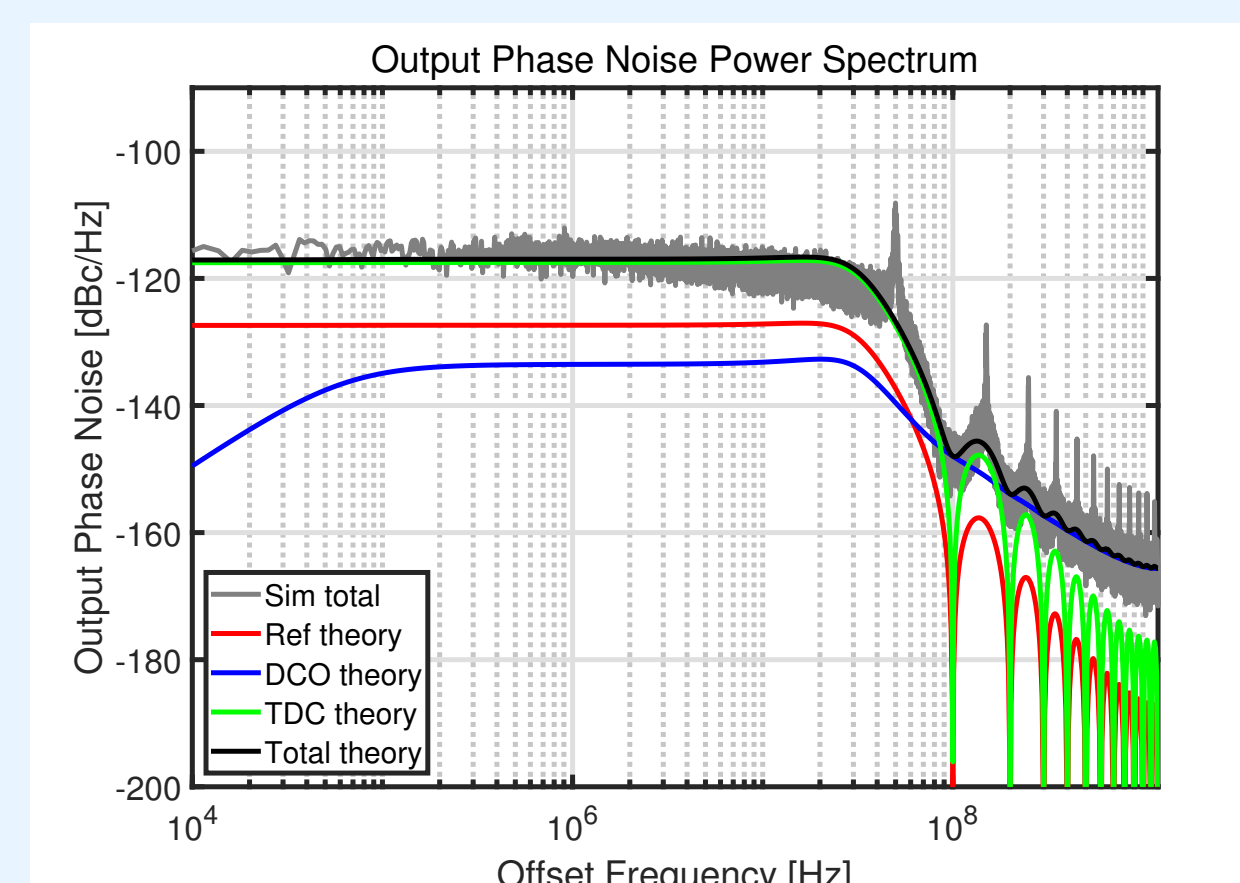
## Stochastic-Resonance-Achieved High Performance



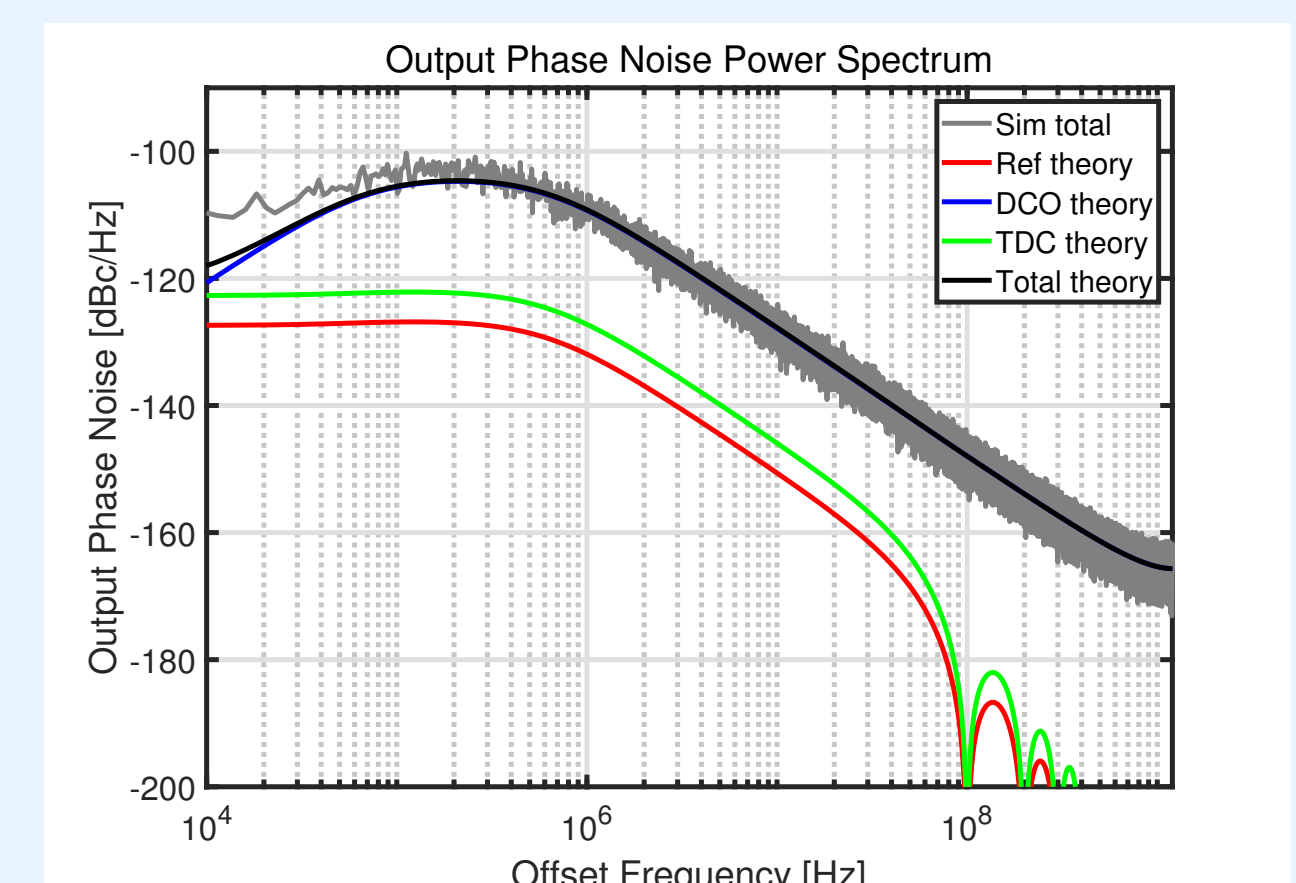
(a) Absence of random noise.



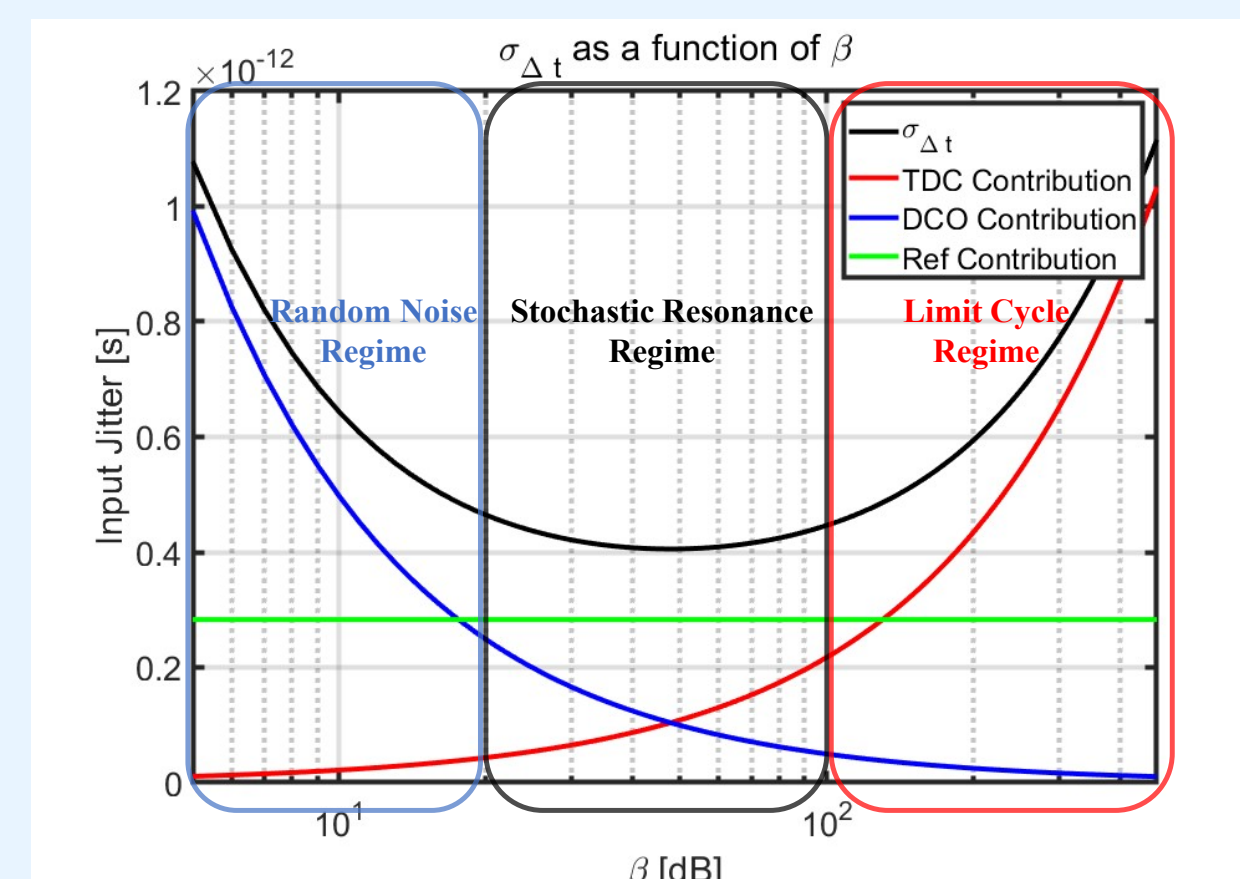
(b) Non-quantized TDC.



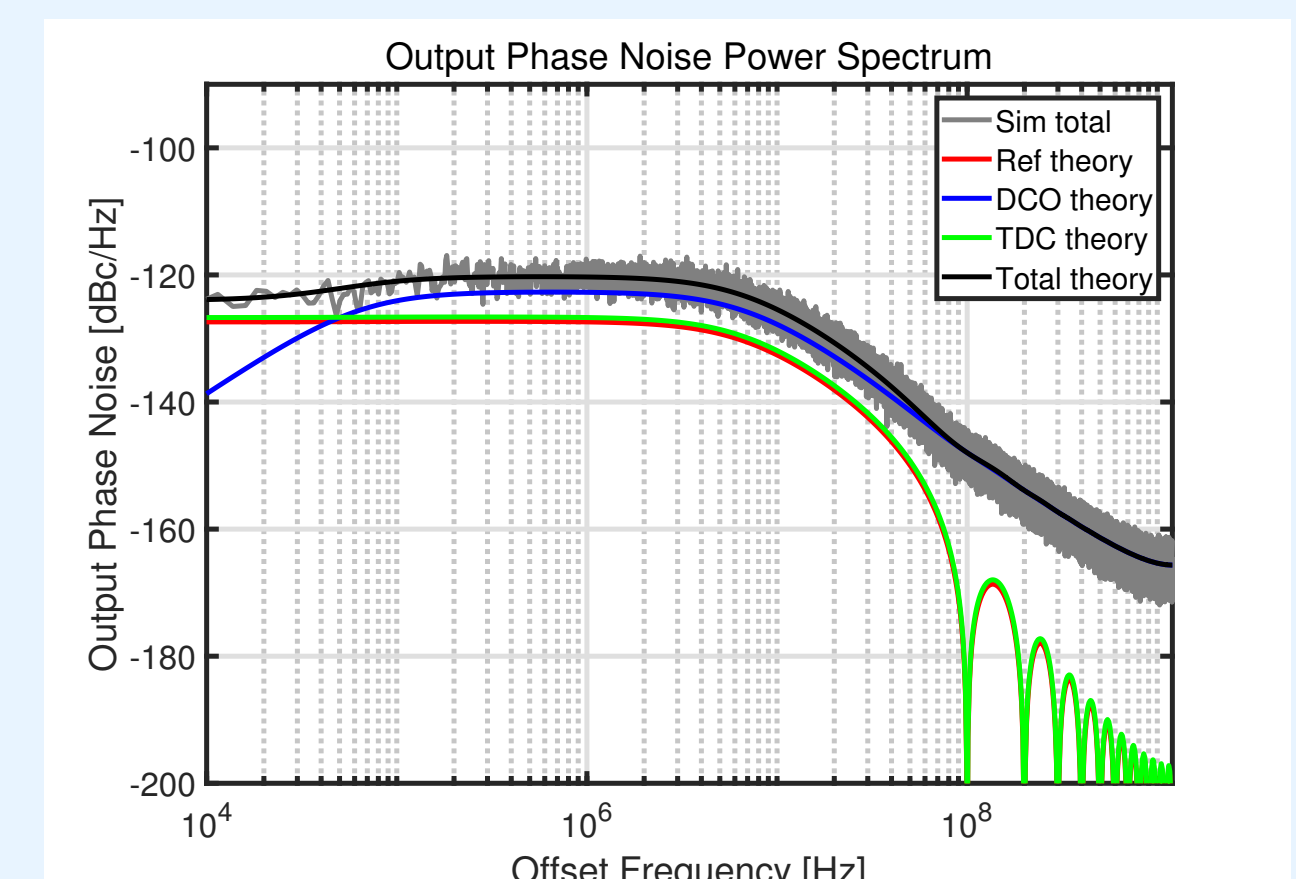
(c)  $\beta = \hat{\beta} \cdot 10$ .



(d)  $\beta = \hat{\beta} / 10$ .



(e) SR configuration.



(f)  $\beta = \hat{\beta}$ .

- (a): In the absence of random noises, the output spectrum consists purely of spurs.
- (b): Considering a linear (non-quantized) TDC, the output spectrum consists purely of PN.
- (c): When  $\beta > \hat{\beta}$ , excess spurs are present at the output.
- (d): When  $\beta < \hat{\beta}$ , excess PN is present at the output.
- (e): Configuration of the SR operation regime.
- (f): When  $\beta = \hat{\beta}$ , the powers of the PN and spurs balance, the system jitter is minimized, and there is no spur in the output spectrum; this is the optimized performance.

## Conclusion & Future Work

We have demonstrated that, by applying the principle of stochastic resonance (SR), the output spurious tones can be randomized and mitigated by the intrinsic random noise throughout digital frequency synthesis to achieve a minimized system jitter and an optimized output spectrum that is spur-free. The literature to date focuses primarily on SR used in integer- $N$  DPLLs. However, the more advanced fractional- $N$  synthesis, where the synthesized frequency is a non-integer multiple of the reference one, yields more quantization-related spurs; this motivates our research into SR techniques to be exploited in the fractional- $N$  mode.

## Key References

- [1] M. D. McDonnell, "Is electrical noise useful? [point of view]," *Proceedings of the IEEE*, vol. 99, no. 2, pp. 242–246, Feb 2011.
- [2] G. Marucci, S. Levantino, P. Maffezzoni, and C. Samori, "Exploiting stochastic resonance to enhance the performance of digital bang-bang PLLs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 10, pp. 632–636, Oct 2013.
- [3] X. Wang and M. P. Kennedy, "Enhanced jitter analysis and minimization for digital PLLs with mid-rise TDCs and its impact on output phase noise," submitted to TCAS I (under review).